

**WHAT IS CLAIMED IS:**

1. A system for increasing effective pulse-width modulated

2 (PWM) drive signal resolution, comprising: /

3       a duty cycle calculator configured to calculate a theoretical  
4 duty cycle for a PWM drive signal to be provided to an associated  
5 power converter based on at least one operating condition thereof,  
6 said theoretical duty cycle not a member of a pre-established set  
7 of allowable duty cycles; and

8       a duty cycle approximator coupled to said duty cycle  
9 calculator and configured to generate a sequence of members of the  
10 set of allowable duty cycles, wherein the sequence at least  
11 approximately averages to said theoretical duty cycle.

2. The system as recited in Claim 1 wherein said at least

2 one operating condition is selected from the group consisting of:

3       input current,

4       input voltage,

5       output current, and

6       output voltage.

3. The system as recited in Claim 1 wherein said set of

2 allowable duty cycles contains only integers.

4. The system as recited in Claim 3 wherein a length of said  
2 sequence is at least approximately proportional to a reciprocal of  
3 a fractional part of said theoretical duty cycle.

5. The system as recited in Claim 1 wherein said set of  
2 allowable duty cycles contains only members chosen as a function of  
3 a relationship between a clock rate and an interval of said PWM  
4 drive signal.

6. The system as recited in Claim 1 wherein said duty cycle  
2 calculator and said duty cycle approximator are implemented in a  
3 processor and said duty cycle approximator provides said sequence  
4 of allowable duty cycles to a comparator coupled to said processor.

7. The system as recited in Claim 1 wherein said sequence of  
2 allowable duty cycles contains only allowable duty cycles  
3 immediately greater than and immediately less than said theoretical  
4 duty cycle.

8. A method of increasing effective pulse-width modulated  
2 drive signal resolution, comprising:

3 calculating a theoretical duty cycle for a PWM drive signal to  
4 be provided to an associated power converter based on at least one  
5 operating condition thereof, said theoretical duty cycle not a  
6 member of a pre-established set of allowable duty cycles; and

7 generating a sequence of members of the set of allowable duty  
8 cycles, wherein the sequence at least approximately averages to  
9 said theoretical duty cycle.

9. The method as recited in Claim 8 wherein said at least  
2 one operating condition is selected from the group consisting of:

3 input current,  
4 input voltage,  
5 output current, and  
6 output voltage.

10. The method as recited in Claim 8 wherein said set of  
2 allowable duty cycles contains only integers.

11. The method as recited in Claim 10 wherein a length of  
2 said sequence is at least approximately proportional to a  
3 reciprocal of a fractional part of said theoretical duty cycle.

12. The method as recited in Claim 8 wherein said set of  
2 allowable duty cycles contains only members chosen as a function of  
3 a relationship between a clock rate and an interval of said PWM  
4 drive signal.

13. The method as recited in Claim 8 wherein said calculating  
2 and said generating are carried out in a processor and said  
3 generating comprises providing said sequence of allowable duty  
4 cycles to a comparator coupled to said processor.

14. The method as recited in Claim 8 wherein said sequence of  
2 allowable duty cycles contains only allowable duty cycles  
3 immediately greater than and immediately less than said theoretical  
4 duty cycle.

15. A power converter, comprising: /

2       at least one power switch interposing at least two input lines  
3       and at least two output lines; and

4       a converter controller for providing a PWM drive signal to  
5       said at least one power switch, including:

6            a duty cycle calculator configured to calculate a  
7       theoretical duty cycle for said PWM drive signal based on at  
8       least one operating condition of said power converter, said  
9       theoretical duty cycle not a member of a pre-established set  
10      of allowable duty cycles, and

11          a duty cycle approximator coupled to said duty cycle  
12       calculator and configured to generate a sequence of members  
13       of the set of allowable duty cycles, wherein the sequence  
14       at least approximately averages to said theoretical duty  
15       cycle.

16. The power converter as recited in Claim 15 wherein said

2       at least one operating condition is selected from the group  
3       consisting of:

4            input current,

5            input voltage,

6            output current, and

7            output voltage.

17. The power converter as recited in Claim 15 wherein said  
2 set of allowable duty cycles contains only integers.

18. The power converter as recited in Claim 17 wherein a  
2 length of said sequence is at least approximately proportional to  
3 a reciprocal of a fractional part of said theoretical duty cycle.

19. The power converter as recited in Claim 15 wherein said  
2 set of allowable duty cycles contains only members chosen as a  
3 function of a relationship between a clock rate and an interval of  
4 said PWM drive signal.

20. The power converter as recited in Claim 15 wherein said  
2 duty cycle calculator and said duty cycle approximator are  
3 implemented in a processor and said duty cycle approximator  
4 provides said sequence of allowable duty cycles to a comparator  
5 coupled to said processor.

21. The power converter as recited in Claim 15 wherein said  
2 sequence of allowable duty cycles contains only allowable duty  
3 cycles immediately greater than and immediately less than said  
4 theoretical duty cycle.